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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/756,436 | 01/12/2004 | Christopher Alan Greer | 200312141-1 | 2182 |

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

| EXAMINER | |
|---|---|
| KIM, DANIEL Y | |
| **ART UNIT** | **PAPER NUMBER** |
| 2185 | |

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/756,436 | GREER ET AL. | |
| | Examiner | Art Unit | |
| | Daniel Kim | 2185 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,4-12,14-18,20 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-12,14-18,20 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. This Office Action is in response to applicant's communication filed July 8, 2006 in response to the PTO Office Action mailed April 4, 2006. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, claims 1, 8 and 18 have been amended, claims 2-3, 13 and 19 have been cancelled, and no other claims have been added. Claims 1, 4-12, 14-18 and 20-21 remain pending in this application.

### *Response to Arguments*

3. Applicant's arguments with respect to claims 1, 4-12, 14-18 and 20-21 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4-7, 17-18 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuskin (US Patent No. 6,829,683) and Glasco (US PGPub No. 20050033924).

For claim 1, Kuskin discloses a method of transferring ownership of a cache line between processors in a shared memory multi-processor computer system, comprising sending a request transaction for ownership of a cache line from a first processor to a memory unit (a method for transferring ownership of data in a distributed shared memory system that includes generating a return request at a processor to return a cache line, col. 1, lines 38-41),

determining from the memory unit which one of a plurality of processors other than the first processor has ownership of the requested cache line and sending a recall transaction to a second processor (a memory directory interface unit determines which processors in the system maintain a copy of the cache line, col. 26, lines 34-35), and

sending the requested cache line with ownership from the second processor to the first processor in response to the recall transaction to a second processor (a processor may request data from any memory within the system through accesses to the memory directory interface unit corresponding to the memory containing the data, and if the data is held in the cache of another processor, the data may be retrieved from the other processor according to a protocol scheme, col. 2, lines 63-67 and col. 3, lines 1-2).

Kuskin fails to disclose the remaining claim limitations.

Glasco, however, helps disclose sending a response transaction from the first processor to the memory unit to confirm receipt of the requested cache line by the first processor (the processor can then send a done response to the memory controller, par. 0050; after receiving the fetched data, a processor may send a source done response to the cache coherence controller, and the transaction is now complete at the requesting cluster, and cache coherence controller in turn sends a source done message to memory controller, upon receiving the source done message, the memory controller can unlock the memory line and the transaction at the home cluster is now complete), and

sending a response transaction from the second processor to the memory unit to confirm that the second processor has sent the requested cache line to the first processor (par. 0050, 0064; the cache coherence controller is configured to receive a cache access request associated with a memory line from a first processor amongst the plurality of processors, obtain response information for the cache access request from a remote data cache associated with the cache coherence controller and provide response information with a completion indicator to the processor, par. 0010).

Kuskin and Glasco are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include sending response transactions indicating completion of the sending and receiving of a requested cache line because this would allow the memory controller to unlock the

memory line for subsequent requests (par. 0050), so that other processors can access the unlocked memory line (par. 0064), as taught by Glasco.

For claim 4, the combined teachings of Kuskin and Glasco disclose the invention as per rejection of claim 1 above.

These teachings further help disclose the response transaction from the second processor to the memory unit includes a copy of the data on the requested cache line (Kuskin: col. 2, lines 63-67 and col. 3, lines 1-2; Glasco: par. 0010, 0050, 0064).

For claim 5, the combined teachings of Kuskin and Glasco disclose the invention as per rejection of claim 1 above.

Kuskin further helps disclose the response transaction from the second processor to the memory unit includes a copy of the data for the requested cache line only when the request for ownership of the cache line from the first processor does not include a guarantee that the first processor will make the requested cache line data available in response to a subsequent request for ownership of the cache line from a third processor (if there is a writeback or relinquish outstanding, no intervention response needs to be issued because the presence of the writeback or relinquish indicates that the processor no longer holds the cache line, col. 22, lines 1-4; if a processor drops a cache line, the rest of the system does not become aware of the dropping of the cache line and interventions for the cache line will continue until a relinquish message is sent to let the system know that a processor is giving up ownership of the cache line, col. 25, lines 24-30).

For claim 6, the combined teachings of Kuskin and Glasco disclose the invention as per rejection of claim 1 above.

Kuskin further helps disclose updating a tag in the memory unit to reflect transfer of ownership of the cache line to the first processor (the state of remotely held copies of a cache line is maintained at the remote locations using a cache to hold the current copy of the cache line, its address tag, and its current state, col. 3, lines 57-60).

For claim 7, the combined teachings of Kuskin and Glasco disclose the invention as per rejection of claim 1 above.

Kuskin further helps disclose the computer system uses a directory-based cache coherency scheme (a non-blocking request/reply protocol scheme preferably optimized for cache coherence implementation, col. 3, lines 49-51; a memory directory interface unit may provide a communication link with one or more local memory devices, col. 2, lines 41-43).

For claim 17, Kustkin discloses a method of transferring ownership of a cache line between processors in a shared memory multi-processor computer system that uses a directory-based cache coherency scheme (the present invention relates to multi-processor computer systems and more particularly to a system and method for transferring ownership of data in a distributed shared memory system, col. 1, lines 12-15; col. 3, lines 49-51; col. 2, lines 41-43), comprising

sending a request transaction for ownership of a cache line from a first processor to a memory unit (col. 1, lines 38-41),

determining from the memory unit which one of a plurality of processors other than the first processor has ownership of the requested cache line and sending a recall transaction to the processor with ownership (col. 26, lines 34-35),

sending the requested cache line with ownership from the processor with ownership to the first processor in response to the recall transaction (col. 2, lines 63-67, col. 3, lines 1-2), and

updating a tag in the memory unit to reflect transfer of ownership of the cache line to the first processor (col. 3, lines 57-60).

Kuskin fails to disclose the remaining claim limitations.

Glasco, however, helps disclose sending a response transaction including a copy of the data for the requested cache line from the processor with ownership to the memory unit to confirm that the processor with ownership has sent the requested cache line to the first processor (par. 0010, 0050, 0064), and

sending a response transaction from the first processor to the memory unit to confirm receipt of the requested cache line by the first processor (par. 0010, 0050, 0064).

Kuskin and Glasco are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include sending response transactions indicating completion of the sending and receiving of a requested cache line because this would allow the memory controller to unlock the

memory line for subsequent requests (par. 0050), so that other processors can access the unlocked memory line (par. 0064), as taught by Glasco.

For claim 18, Kuskin discloses an apparatus for transferring ownership of a cache line between a plurality of processors in a multi-processor computer system with a shared memory unit (col. 1, lines 12-15), comprising

a first transaction line for providing a request transaction for ownership of a cache line from a first processor to the shared memory unit (col. 1, lines 38-41),

a second transaction line for providing a recall transaction to a second processor after determining from the shared memory unit which one of the plurality of processors other than the first processor has ownership of the requested cache line (col. 26, lines 34-35), and

a third transaction line for providing transfer of the requested cache line from the second processor to the first processor in response to the recall transaction (col. 2, lines 63-67, col. 3, lines 1-2).

Kuskin fails to disclose the remaining claim limitations.

Glasco, however, helps disclose a fourth transaction line for providing a response transaction from the first processor to the shared memory unit to confirm receipt of ownership of the requested cache line by the first processor (par. 0010, 0050, 0064), and

a fifth transaction line for providing a response transaction from the second processor to the memory unit to confirm transfer of the requested cache line from the second processor to the first processor (par. 0010, 0050, 0064).

Kuskin and Glasco are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include sending response transactions indicating completion of the sending and receiving of a requested cache line because this would allow the memory controller to unlock the memory line for subsequent requests (par. 0050), so that other processors can access the unlocked memory line (par. 0064), as taught by Glasco.

For claim 20, the combined teachings of Kuskin, Glasco and McCracken disclose the invention as per rejection of claim 18 above.

These teachings further help disclose a fifth transaction line for providing a response transaction from the second processor to the memory unit to confirm transfer of the requested cache line from the second processor to the first processor together with a copy of the requested cache line data (Kuskin: col. 2, lines 63-67 and col. 3, lines 1-2; Glasco: par. 0010, 0050, 0064).

For claim 21, the combined teachings of Kuskin, Glasco and McCracken disclose the invention as per rejection of claim 18 above.

Kuskin further helps disclose the computer system uses a directory-based cache coherency scheme (col. 3, lines 49-51; col. 2, lines 41-43).

6. Claims 8-12 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuskin (US Patent No. 6,829,683), Glasco (US PGPub No. 20050033924) and McCracken (US Patent No. 6,381,681).

For claim 8, the combined teachings of Kuskin and Glasco disclose the invention as per rejection of claims 1 and 2 above. These teachings, however, fail to disclose these steps for processors and cache lines that are contained within cell divisions.

McCracken, however, helps disclose each cell of a shared memory multiprocessor system may include any suitable number of processors and clusters, each representative processor includes an associated cache and is coupled to a memory controller through which it acquires access to memory pages, each memory page has a set of cache lines available for acquisition by other processors so that other processors may share memory pages, and each memory page includes a memory data and a memory directory which tracks information related to a memory page such as the current state of each cache line, what processors are associated with cache lines, and other memory information (col. 3, lines 20-32).

Kuskin, Glasco and McCracken are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include cell divisions because this would allow for separate acquire and release protection and because memory updates from processors within a cell common to a shared memory page being updated may occur immediately and reduce processing overhead associated with memory coherency (col. 2, lines 29-40), as taught by McCracken.

For claim 9, the combined teachings of Kuskin, Glasco and McCracken disclose the invention as per rejection of claim 8 above.

McCracken further discloses a method wherein m = n = p (the multiprocessor system may include any suitable number of processors and any suitable number of cells, col. 3, lines 15-16; each cell may include any suitable number of processors, col. 3, lines 20-21).

For claim 10, the combined teachings of Kuskin, Glasco and McCracken disclose the invention as per rejection of claim 8 above.

McCracken further helps disclose m = n (col. 3, lines 15-16, 20-21).

For claim 11, the combined teachings of Kuskin, Glasco and McCracken disclose the invention as per rejection of claim 8 above.

McCracken further helps disclose m = p (col. 3, lines 15-16, 20-21).

For claim 12, the combined teachings of Kuskin, Glasco and McCracken disclose the invention as per rejection of claim 8 above.

McCracken further helps disclose n = p (col. 3, lines 15-16, 20-21).

For claim 14, the combined teachings of Kuskin, Glasco and McCracken disclose the invention as per rejection of claim 8 above.

These teachings further help disclose the response transaction from the processor with ownership to the memory unit includes a copy of the data for the requested cache line (Kuskin: col. 2, lines 63-67 and col. 3, lines 1-2; Glasco: par. 0010, 0050, 0064).

For claim 15, the combined teachings of Kuskin, Glasco and McCracken disclose the invention as per rejection of claim 8 above.

Kuskin further helps disclose the response transaction from the processor with ownership to the memory unit includes a copy of the data for the requested cache line only when the request for ownership of the cache line from the first processor does not include a guarantee that the first processor will make the requested cache line data available in response to a subsequent request for ownership of the cache line from a third processor (col. 22, lines 1-4; col. 25, lines 24-30).

For claim 16, the combined teachings of Kuskin, Glasco and McCracken disclose the invention as per rejection of claim 8 above.

Kuskin further helps disclose updating a tag in the memory unit to reflect transfer of ownership of the cache line to the first processor (col. 3, lines 57-60).

***Citation of Pertinent Prior Art***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McAllister et al (US PGPub No. 20030056068) discloses a memory controller generating a transaction requesting one of the data lines to one of a plurality of modules when the module has a private or shared copy of the data line, and returning the data line or a response indicating that no copy of the line exists, and a code identifying the module requesting the data line.

Baumgartner et al (US Patent No. 6,275,907) discloses cache hierarchies that hold copies of requested cache lines as indicated by coherency responses received in

request transactions in a non-uniform memory access computer system with a plurality of processing nodes and a node interconnect.

Gaither et al (US Patent No. 6,868,481) discloses a computer system maintains a list of a global ownership tag list for all cache lines in the eystem for which a cache has ownership, and that lines may be requested and shareable by devices.

Okochi et al (US PGPub No. 20040024839) discloses a multiprocessor system in which transactions may request a data transfer or invalidate cache data, and sending of data in response to a data transfer request.

***Contact Information***

8. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 10:00am-6:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah, is also reachable at 571-272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

9-11-06

SANJIV SHAH
PRIMARY EXAMINER